

What Is Claimed Is:

1 1. A method of fabricating a pair of single-poly EPROM cells,
2 compatible with CMOS process, comprising:
3 providing a substrate with an isolation region to define
4 a striped active area;
5 forming a deep well of first conductive type located under
6 the isolation region and the striped active area;
7 forming a gate oxide layer on the striped active area;
8 forming a conductive layer on the substrate having the gate
9 oxide layer formed thereon;
10 defining the conductive layer to form a pair of floating
11 gates and a pair of selective gates, with a gap between the pair
12 of floating gates and the pair of selective gates, wherein the
13 pair of selective gates are striped and perpendicular to the
14 striped active area, and the pair of selective gates are disposed
15 between the pair of floating gates;
16 forming a well of second conductive type in the deep well
17 of first conductive type below the pair of selective gates and
18 the pair of floating gates;
19 forming a pair of sources in the side walls of the well
20 of second conductive type, the pair of sources connected to each
21 other via the deep well of first conductive type; and
22 forming a drain in the well of second conductive type between
23 the pair of selective gates.

1 2. The method of claim 1, wherein the isolation region is
2 a field oxide layer.

1 3. The method of claim 1, wherein the isolation region is
2 a shallow trench isolation.

1 4. The method of claim 1, wherein the conductive layer is
2 a polysilicon layer.

1 5. The method of claim 1, wherein the method of forming
2 the pair of floating gates and the pair of selective gates
3 comprises:

4 forming a mask layer on the conductive layer, the mask layer
5 substantially having the pattern of the pair of floating gates
6 and the pair of selective gates;

7 forming a plurality of spacers on the side walls of the
8 mask layer, wherein the width of the gap between the pair of
9 floating gates and the pair of selective gates is controlled
10 by the spacers; and

11 etching the conductive layer using the mask layer's spacers
12 as an etching mask.

1 6. The method of claim 5, wherein the method of forming
2 the well of second conductive type comprises:

3 forming a photoresist layer on the substrate on which the
4 mask layer and the spacers are formed, the photoresist layer
5 substantially having a pattern corresponding to the drain and
6 being parallel to pair of selective gates;

7 implanting dopants of second conductive type in the deep
8 well of first conductive type using the photoresist layer as
9 a mask;

10 removing the photoresist layer;

11 thermally driving the dopants so as to form the striped
12 well of second conductive type disposed under the pair of floating
13 gates; and

14 removing the mask layer and the spacers.

1 7. The method of claim 1, wherein the step of forming the
2 sources further comprising forming a dielectric layer on the

3 surface of the conductive layer to fill the gap between the pair
4 of floating gates and the pair of selective gates.

1 8. A structure of single-poly EPROM which is suitable for
2 using as memory cell in a substrate, comprising:

3 an isolation region disposed in the substrate to define
4 a striped active area;

5 a deep well of first conductive type located under the
6 isolation region and the striped active area;

7 a gate oxide layer disposed on the striped active area on
8 the substrate;

9 a pair of selective gates disposed on the gate oxide layer
10 and the isolation region, wherein the pair of selective gates
11 are striped and perpendicular to the striped active area;

12 a pair of floating gates disposed on the gate oxide layer,
13 and are corresponding to the active area, wherein a gap is formed
14 between the pair of floating gates and the pair of selective
15 gates;

16 a well of second conductive type disposed in the deep well
17 of first conductive type below the pair of selective gates and
18 the pair of floating gates;

19 a pair of sources disposed on both sides of the well of
20 second conductive type, the pair of sources connected to each
21 other via the deep well of first conductive type; and

22 a drain disposed in the well of second conductive type
23 between the pair of selective gates.

1 9. The structure of claim 8, wherein the isolation region
2 is a field oxide layer.

1 10. The structure of claim 8, wherein the isolation region
2 is a shallow trench isolation.

1 11. The structure of claim 8, wherein the pair of floating
2 gates and the pair of selective gates are polysilicon.

1 12. The structure of claim 8, wherein the pair of sources
2 are laterally extended to half the width of the pair of floating
3 gates.

1 13. A method for programming memory cells of a single-poly
2 EPROM, wherein a pair of memory cells share a drain, the structure
3 thereof comprising:

4 an isolation region disposed in the substrate to define
5 a striped active area;

6 a deep well of first conductive type located under the
7 isolation region and the striped active area;

8 a gate oxide layer disposed on the substrate at the striped
9 active area;

10 a pair of selective gates disposed on the gate oxide layer
11 and the isolation region, wherein the pair of selective gates
12 are striped and perpendicular to the striped active area;

13 a pair of floating gates disposed on the gate oxide layer
14 and are corresponding to the active area, wherein a gap is formed
15 between the pair of floating gates and the pair of selective
16 gates;

17 a well of second conductive type disposed in the deep well
18 of first conductive type below the pair of selective gates and
19 portions of the pair of floating gates;

20 a pair of sources disposed on both sides of the well of
21 second conductive type, wherein the pair of sources are connected
22 to each other via the deep well of first conductive type; and

23 a drain disposed in the well of second conductive type
24 between the pair of selective gates;

25 the method of applying programming bias voltages to a
26 selected memory cell comprising the following steps:

27 applying a first positive voltage to the selective gate
28 of the selected memory cell, the first positive voltage being
29 about 1.5-2 V;

30 applying a second positive voltage to the pair of sources,
31 the second positive voltage being about 10-12 V;
32 grounding the well of second conductive type;
33 grounding the drain; and
34 grounding the selective gate of the other unselected memory
35 cell,

36 wherein the programming bias voltages cause or make charge
37 carriers to perform source side injection (SSI), and accumulate
38 in the floating gate of the selected memory cell.

1 14. A method for reading memory cell of a single-poly EPROM,
2 wherein a pair of memory cells share a drain, the structure
3 comprising:

4 an isolation region disposed in the substrate to define
5 a striped active area;

6 a deep well of first conductive type located under the
7 isolation region and the striped active area;

8 a gate oxide layer disposed on the striped active area on
9 the substrate;

10 a pair of selective gates disposed on the gate oxide layer
11 and the isolation region, wherein the pair of selective gates
12 are striped and perpendicular to the striped active area;

13 a pair of floating gates disposed on the gate oxide layer
14 and are corresponding to the active area, wherein a gap is formed
15 between the pair of floating gates and the pair of selective
16 gates;

17 a well of second conductive type disposed in the deep well
18 of first conductive type below the pair of selective gates and
19 portions of the pair of floating gates;

20 a pair of sources disposed on both sides of the well of
21 second conductive type, the pair of sources being connected to
22 each other via the deep well of first conductive type; and
23 a drain disposed in the well of second conductive type
24 between the pair of selective gates,
25 the method of applying reading bias voltages to a selected
26 memory cell comprising the following steps:
27 applying a first positive voltage to the selective gate
28 of the selected memory cell, the first positive voltage being
29 Vcc;
30 applying a second positive voltage to the drain, the second
31 positive voltage being about 2 V; and
32 grounding the selective gate of the other unselected memory
33 cell.